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1 **Computational Efficiency in the Determination of Thévenin and Nort Equivalents**
Director, S.; Wayne, D.;
Circuits and Systems, IEEE Transactions on [legacy, pre - 1988] , Volume: 19 , Issue: 1 , Jan 1972
Pages:96 - 98

[Abstract]   [PDF Full-Text (376 KB)]   **IEEE JNL**

---

2 **Osculating Thevenin model for predicting delay and slew of capaciti characterized cells**
Sheehan, B.N.;
Design Automation Conference, 2002. Proceedings. 39th , 10-14 June 2002
Pages:866 - 869

[Abstract]   [PDF Full-Text (410 KB)]   **IEEE CNF**

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1 Circuit effects in static timing: Osculating Thevenin model for predicting delay and slew ▰
       of capacitively characterized cells
       Bernard N. Sheehan
       June 2002 **Proceedings of the 39th conference on Design automation**

       Full text available: 📄 pdf(76.62 KB)   Additional Information: full citation, abstract, references, index terms

       To extrapolate from one point to another using a line, one had better get the slope right. In
       this paper we apply a similar concept to the important problem in Static Timing Analysis
       (STA) of predicting cell timing for RC loads using capacitive characterization data. Instead
       of a line we have a Thevenin circuit, and instead of matching slopes we match load
       sensitivities. We present a table driven, highly accurate cell delay and slew prediction
       procedure that can improve STA when interconnect eff ...

       Keywords: effective capacitance, static timing analysis

2 The analog behavior of digital integrated circuits   ▰
       Lance A. Glasser
       June 1981 **Proceedings of the eighteenth design automation conference on Design
                 automation**
       Full text available: 📄 pdf(674.15 KB)   Additional Information: full citation, abstract, references, citings, index
                                                                          terms

       The analog behavior of digital VLSI circuits is investigated. A theory based on nonlinear
       Thevenin equivalent circuits and RC ladder networks is developed. We obtain closed form
       expressions for the upper and lower bounds on propagation delay through a string of
       inverters. We generalize this to multiple-input, multiple-output gates and show that the
       problem of estimating signal propagation delays in VLSI circuits may be reduced to the
       problem of summing the step responses of a set of linear ...

3 Computer-generated design of electric circuits   ▰
       Kwa-Sur Tam, Michael Besso, Renuka Racha
       June 1988 **Proceedings of the first international conference on Industrial and
                 engineering applications of artificial intelligence and expert systems -
                 Volume 1**
       Full text available: 📄 pdf(597.11 KB)   Additional Information: full citation, abstract, references, index terms

       An artificial intelligence-based design automation methodology for computer-generated
       design of electric circuit is proposed. Given the requirements of the circuit to be designed, a
       program using this approach can generate a set of candidate circuits, evaluate them
       according to the specified requirements, and recommend the most suitable circuit(s). A

PROLOG program (called VMD) implementing this approach has been developed for the design of voltage multiplier circuits. Issues pertaining to ...

4 Analysis and reliable design of ECL circuits with distributed RLC interconnections
Monjurul Haque, S. Chowdhury
July 1993 **Proceedings of the 30th international on Design automation conference**

Full text available: pdf(502.35 KB) Additional Information: full citation, references, index terms

5 ClariNet: a noise analysis tool for deep submicron design
Rafi Levy, David Blaauw, Gabi Braca, Aurobindo Dasgupta, Amir Grinshpon, Chanlee Oh, Boaz Orshav, Supamas Sirichotiyakul, Vladimir Zolotov
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(101.67 KB) Additional Information: full citation, abstract, references, citings, index terms

Coupled noise analysis has become a critical issue for deep-submicron, high performance design. In this paper, we present, ClariNet, an industrial noise analysis tool, which was developed to efficiently analyze large, high performance processor designs. We present the overall approach and tool flow of ClariNet and discuss three critical large-processor design issues which have received limited discussion in the past. First, we present how the driver gates of a coupled interconnect network a ...

6 Noise propagation and failure criteria for VLSI designs
V. Zolotov, D. Blaauw, S. Sirichotiyakul, M. Becer, C. Oh, R. Panda, A. Grinshpon, R. Levy
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(237.68 KB) Additional Information: full citation, abstract, references, citings, index terms

Noise analysis has become a critical concern in advanced chip designs. Traditional methods suffer from two common issues. First, noise that is propagated through the driver of a net is combined with noise injected by capacitively coupled aggressor nets using linear summation. Since this ignores the non-linear behavior of the driver gate the noise that develops on a net can be significantly underestimated. We therefore propose a new linear model that accurately combines propagated and injected no ...

7 An MOS digital network model on a modified thevenin equivalent for logic simulation
Tsuyoshi Takahashi, Satoshi Kojima, Osamu Yamashiro, Kazuhiko Eguchi, Hideki Fukuda
June 1984 **21st Proceedings of the Design Automation Conference on Design automation**

Full text available: pdf(387.72 KB) Additional Information: full citation, abstract, references, index terms

A novel analytical model of MOS digital networks, which is based on a modified Thevenin equivalent, is described. The model can handle all the primary circuits inherent in MOS technology, such as transistor logics, wired-ORs, tri-state circuits, charge-share operation, and bidirectional pass transistors etc., with precise estimation of delay time. The model has been implemented in a logic/fault simulator, named HASL-GT. Performance of 4 to 10 k events/sec has been obtained on HIT ...

8 Evaluation of parts by mixed-level DC-connected components in logic simulation
Dah-Cherng Yuan, Lawrence T. Pillage, Joseph T. Rahmeh
July 1993 **Proceedings of the 30th international on Design automation conference**

Full text available: pdf(630.26 KB) Additional Information: full citation, references, index terms

9 Circuits for wide-window superscalar processors

Dana S. Henry, Bradley C. Kuszmaul, Gabriel H. Loh, Rahul Sami
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(234.37 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Our program benchmarks and simulations of novel circuits indicate that large-window processors are feasible. Using our redesigned superscalar components, a large-window processor implemented in today's technology can achieve an increase of 10-60% (geometric mean of 31%) in program speed compared to today's processors. The processor operates at clock speeds comparable to today's processors, but achieves significantly higher ILP. To measure the impact of a large window on clock spe ...

10 <u>Coping with RC(L) interconnect design headaches</u>

Lawrence Pileggi
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(96.33 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>
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Physical interconnect effects have a dominant impact on today's deep submicron IC designs. In this tutorial paper we will describe the technology trends which have brought about this interconnect dominance, then consider some of the modeling and analysis approximations available for both pre- and post-layout interconnect design. This coverage will not be an exhaustive summary, but one that is primarily focused on moment-based analysis techniques, from the Elmore delay, to the more recent advance ...

11 <u>VLSI design parsing (preliminary version)</u>

Akhilesh Tyagi
November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(710.09 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

12 <u>Performance improvement with circuit-level speculation</u>

Tong Liu, Shih-Lien Lu
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(121.66 KB)
ps(857.89 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

13 <u>Hierarchical model order reduction for signal-integrity interconnect synthesis</u>

Yu-Min Lee, Charlie Chung-Ping Chen
March 2001 **Proceedings of the 11th Great Lakes Symposium on VLSI**

Full text available: pdf(690.28 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

14 <u>A hardware engine for analogue mode simulation of MOS digital circuits</u>

David M. Lewis
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available: pdf(803.41 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

Purely digital simulators that model digital circuits by approximations often produce poor results with even simple circuits. Analogue simulators, however, are far more accurate than necessary for digital circuits and correspondingly expensive to use. We argue that an

analogue simulation is necessary, but that a simple enough approximation can be used to allow a hardware simulation engine to perform the calculations. The critical features of such an engine are discussed here, its performanc ...

15 Timing metrics for physical design of deep submicron technologies

Lawrence Pileggi
April 1998 **Proceedings of the 1998 international symposium on Physical design**

Full text available: pdf(727.52 KB)   Additional Information: full citation, abstract, references, citings, index terms

Performance-driven physical design is becoming more important as advances in IC technologies enable gigahertz operating frequencies. These same IC technologies, however, exhibit dominant interconnect resistance, non-negligible coupling capacitance, and even the potential for inductance effects, which makes the performance modeling and prediction more difficult. In this tutorial paper we will overview some of the existing timing metrics that are suitable for use during physical desig ...

16 Poster Session 4: Power estimation of sequential circuits using hierarchical colored hardware petri net modeling

Ashok K. Murugavel, N. Ranganathan
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available: pdf(77.11 KB)   Additional Information: full citation, abstract, references, index terms

A Hierarchical Colored Hardware Petri net (HCHPN) based model was proposed in [8] for estimating switching activity in combinational circuits. In this paper, we model sequential circuits as HCHPNs incorporating real delays for both gates and interconnects. Thus, the given sequential circuit is first modeled as a HCHPN and simulated for switching activity estimation in the petri net domain which leads to better accuracy and faster simulation. Experimental results for ISCAS'89 benchmark circuits s ...

17 Energy aware design: Optimizing pipelines for power and performance

Viji Srinivasan, David Brooks, Michael Gschwind, Pradip Bose, Victor Zyuban, Philip N. Strenski, Philip G. Emma
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.24 MB)   Additional Information: full citation, abstract, references, index terms
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During the concept phase and definition of next generation high-end processors, power and performance will need to be weighted appropriately to deliver competitive cost/performance. It is not enough to adopt a CPI-centric view alone in early-stage definition studies. One of the fundamental issues confronting the architect at this stage is the choice of pipeline depth and target frequency. In this paper we present an optimization methodology that starts with an analytical power-performance model ...

18 Low-power physical design: Petri net modeling of gate and interconnect delays for power estimation

Ashok K. Murugavel, N. Ranganathan
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(97.49 KB)   Additional Information: full citation, abstract, references, citings, index terms

In this paper, a new type of Petri net called Hierarchical Colored Hardware Petri net, to model real-delay switching activity for power estimation is proposed. The logic circuit is converted into a HCHPN and simulated as a Petri net to get the switching activity estimate and thus the power values. The method is accurate and is significantly faster than other simulative methods. The HCHPN yields an average error of 4.9% with respect to Hspice for the ISCAS '85 benchmark circuits. The per-pattern ...

19 <u>Determination of worst-case aggressor alignment for delay calculation</u>

Paul D. Gross, Ravishankar Arunachalam, Karthik Rajagopal, Lawrence T. Pileggi

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available: <u>pdf(883.15 KB)</u>   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

20 <u>AWEsymbolic: compiled analysis of linear(ized) circuits using asymptotic waveform evaluation</u>

J. Y. Lee, R. A. Rohrer

July 1992   **Proceedings of the 29th ACM/IEEE conference on Design automation conference**

Full text available: <u>pdf(575.80 KB)</u>   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

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980551, B76045306; 760000.

Title
A computing aid for transistorized **circuit design.**

Author(s)
Rauch-V.

Author affiliation
Elektrotech Fakulta CVUT, Praha, Czechoslovakia.

Source
Slaboproudy-Obzor (Czechoslovakia), vol.37, no.8, p.376-81, Aug. 1976.

CODEN
SLOZAE.

ISSN
ISSN: 0037-668X.

Publication year
1976.

Language
CZ.

Publication type
J Journal Paper.

Treatment codes
T Theoretical or Mathematical.

Abstract
Contains the instructions for a unified computation of the **Thevenin** equivalent of a transistor or electronic tube **circuit** using a triangular aid. This enables the required formulae to be set up according to a unified rule, in which the respective expressions are interchanged cyclically according to the electrode to which the computation is related. (3 refs).

Descriptors
bipolar-transistors; design-aids; equivalent-circuits; linear-network-synthesis.

Keywords
triangular aid; computing aid for transistorised **circuit design;** unified computation of **Thevenin** equivalent; expressions interchanged cyclically; electronic **circuit design.**

Classification codes

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B1130     (General analysis and synthesis methods).
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Accession number & update
     5908987, C9806-5610S-004; 980512.
Title
     Termination techniques for high-speed buses.
Author(s)
     Ethirajan-K; Nemec-J.
Author affiliation
     California Micro Devices, Milpitas, CA, USA.
Source
     EDN (US Edition)(USA), vol.43, no.4, p.135-40, 142, 144-5, 16 Feb. 1998. , Published: Cahners
     Publishing.
CODEN
     EDNEFD.
ISSN
     ISSN: 0012-7515.
Availability
     SICI: 0012-7515(19980216)43:4L.135:TTHS; 1-Y.
Publication year
     1998.
Language
     EN.
Publication type
     J Journal Paper.
Treatment codes
     P Practical.

Abstract
     Choosing the proper bus-termination technique-parallel, series, **Thevenin,** ac, or diode-based-is
     critical to digital-system performance. Improper termination can lead to ringing and stair-stepping,
     which in turn can cause false triggering and data errors. Common passive-termination techniques
     include parallel, **Thevenin,** series, and ac terminations. Schottky-diode termination, which is an
     unconventional passive-termination technique, also provides some advantages. Familiarity with each
     technique's relative merits and demerits helps you choose the best technique or techniques for your
     board or system. (20 refs).

Descriptors
     digital-systems; printed-circuit-design; system-buses.
Keywords
     high speed buses; bus termination technique; parallel techniques; series techniques; **Thevenin**
     techniqes; diode based techniques; PC **design;** digital system performance.
Classification codes

     C5610S (System buses).
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L6: Entry 1 of 1   File: USPT   Jan 3, 1995

US-PAT-NO: 5379231
DOCUMENT-IDENTIFIER: US 5379231 A
** See image for Certificate of Correction **

TITLE: Method and apparatus for simulating a microelectric interconnect circuit

DATE-ISSUED: January 3, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pillage; Lawrence T.	Austin	TX		
Ratzlaff; Curtis L.	Austin	TX		
Gopal; Nanda	Austin	TX		

US-CL-CURRENT: 703/14; 716/1

| Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D |

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PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040073264 A1

TITLE: Method for monitoring end of life for battery

PUBLICATION-DATE: April 15, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lyden, Michael J.	Shoreview	MN	US	

US-CL-CURRENT: 607/7

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

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PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040024426 A1

TITLE: Method for monitoring end of life for battery

PUBLICATION-DATE: February 5, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lyden, Michael J.	Shoreview	MN	US	

US-CL-CURRENT: 607/27

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PGPUB-DOCUMENT-NUMBER: 20030174083
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030174083 A1

TITLE: Methods and apparatus for analog-to-digital conversion

PUBLICATION-DATE: September 18, 2003

INVENTOR-INFORMATION:
NAME   CITY   STATE   COUNTRY   RULE-47
Mayfield, Glenn A   West Lafayette   IN   US

US-CL-CURRENT: 341/166

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PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020140404 A1

TITLE: Method for monitoring end of life for battery

PUBLICATION-DATE: October 3, 2002

INVENTOR-INFORMATION:
NAME   CITY   STATE   COUNTRY   RULE-47
Lyden, Michael J.   Shoreview   MN   US

US-CL-CURRENT: 320/166

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

□ 5. Document ID: US 20010034541 A1

L5: Entry 5 of 9   File: PGPB   Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034541
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034541 A1

TITLE: Method for monitoring end of life for battery

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:
NAME   CITY   STATE   COUNTRY   RULE-47
Lyden, Michael J.   Shoreview   MN   US

US-CL-CURRENT: 607/29

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐   6.   Document ID: US 6732065 B1

L5: Entry 6 of 9   File: USPT   May 4, 2004

US-PAT-NO: 6732065
DOCUMENT-IDENTIFIER: US 6732065 B1

TITLE: Noise estimation for coupled RC interconnects in deep submicron integrated circuits

DATE-ISSUED: May 4, 2004

INVENTOR-INFORMATION:
| NAME | CITY | STATE | ZIP CODE | COUNTRY |
| Muddu; Sudhakar | Santa Clara | CA | | |

US-CL-CURRENT: 703/2; 703/13, 703/14, 716/5, 716/6

| Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De |

☐   7.   Document ID: US 6654640 B2

L5: Entry 7 of 9   File: USPT   Nov 25, 2003

US-PAT-NO: 6654640
DOCUMENT-IDENTIFIER: US 6654640 B2
** See image for Certificate of Correction **

TITLE: Method for monitoring end of life for battery

DATE-ISSUED: November 25, 2003

INVENTOR-INFORMATION:
| NAME | CITY | STATE | ZIP CODE | COUNTRY |
| Lyden; Michael J. | Shoreview | MN | | |

US-CL-CURRENT: 607/29

| Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De |

☐   8.   Document ID: US 6631293 B2

L5: Entry 8 of 9   File: USPT   Oct 7, 2003

US-PAT-NO: 6631293
DOCUMENT-IDENTIFIER: US 6631293 B2
** See image for Certificate of Correction **

TITLE: Method for monitoring end of life for battery

DATE-ISSUED: October 7, 2003

INVENTOR-INFORMATION:
NAME	CITY	STATE	ZIP CODE	COUNTRY
Lyden; Michael J.	Shoreview	MN		

US-CL-CURRENT: 607/29

| Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D |

☐ 9. Document ID: US 5379231 A

L5: Entry 9 of 9   File: USPT   Jan 3, 1995

US-PAT-NO: 5379231
DOCUMENT-IDENTIFIER: US 5379231 A
** See image for Certificate of Correction **

TITLE: Method and apparatus for simulating a microelectric interconnect circuit

DATE-ISSUED: January 3, 1995

INVENTOR-INFORMATION:
NAME	CITY	STATE	ZIP CODE	COUNTRY
Pillage; Lawrence T.	Austin	TX		
Ratzlaff; Curtis L.	Austin	TX		
Gopal; Nanda	Austin	TX		

US-CL-CURRENT: 703/14; 716/1

| Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D |

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